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LOT: 82 VIDEO CODEC AND COMPUTATIONAL ENGINE CHIP TECHNOLOGY LOT FOR SALE | OCEAN TOMO

LOT: 82视频编解码和计算引擎芯片技术专利包待售 | OCEAN TOMO

Ocean Tomo Bid-Ask(TM) Market patent auction lot number 82, consists of nine published patents. The technology creates a video encoder/compression supercomputer on a chip with extremely low power dissipation of 70 mW and the shortest possible latency at 698 uSec. Though the patented architecture and massive parallelism computing technology currently encodes video using the H.264 standard, it is extensible to more advanced and computationally demanding standards.

Ocean Tomo Bid Ask™市场上待拍的82号专利包，包含九项已公布的专利。该技术在芯片上实现用于视频编码/压缩的超级计算机，只需70mW的极低能耗和 698微妙的最短延时。目前，专利架构适行H.264标准，并可扩展至更高级的计算标准。

For further information or to bid on this lot, please email Bid-Ask@OceanTomo.com.

竞拍该专利包或详询更多信息，欢迎联系 Bid-Ask@OceanTomo.com.

NO.	PUBLICATION NUMBER	TITLE	PRIMARY IP CLASS	FILE DATE	PRIORITY DATE	PUBLICATION DATE	FORWARD CITATIONS
序号	公开号	专利名称	IPC主分类号	申请日	优先权日	公开日	引证数量
1	US8566515	Memory subsystem 内存子系统	G09G00536000	2009-02-26	2009-01-12	2013-10-22	8
2	US8660193	Parallel, pipelined, integrated–circuit implementation of a computational engine 计算引擎的并行流水线式集成电路实现	H04N00718000	2009-02-04	2009-01-12	2014-02-25	8
3	US8503534	Multi–bus architecture for a video codec 视频编解码器的多总线架构	H04B00166000	2010-04-22	2010-04-22	2013-08-06	2
4	DE102011002098 A1	Multi – bus – architecture for a video – codec 视频编解码器的多总线架构	H04N00726000	2011-04-15	2010-04-22	2011-10-27	0
5	DE112009004320 T5	Memory – subsystem 内存 – 子系统	G06T00160000	2009-12-21	2009-01-12	2012-02-02	0
6	DE112009004344 T8	Parallel implementation of a computer according to the pipeline process on an integrated circuit 计算引擎的并行流水线式集成电路实现	G06F01516700	2009-12-21	2009-01-12	2012-08-23	0
7	CN102369552 B	Memory subsystem 内存子系统	G06F01202000	2009-12-21	2009-01-12	2014-11-05	0
8	CN102238383 B	In video coding and decoding device a bus system structure 视频编解码装置的总线系统架构	H04N01917600	2011-04-21	2010-04-22	2016-01-06	0
9	CN102369522 A	Parallel, pipelined, integrated–circuit implementation of a computational engine 计算引擎的并行流水线式集成电路实现	G06F01580000	2009-12-21	2009-01-12	2016-04-20	0