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# LOW POWER LOW LATENCY VIDEO CODEC – LOT 82





**BRING**  
TECHNOLOGY

Architected  
Performance

# SUPER COMPUTING WITHIN A CHIP

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- Extreme application architecture
- Shattering paradigms
  - Ultra wide bus
  - Massive parallelism
  - Distributed memory
- Current design
  - Video Encoder – Code name: Eagle
- Although our patented architecture currently encodes video using the H.264 standard, it is extensible to more advanced and computationally demanding standards

# SHATTERING PARADIGMS

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- **EAGLE'S SUPER LARGE WORD SIZE**
  - Eagle - Main object bus is 3,072 bits wide
  - Commercial microprocessor - 32 or 64 bits wide
    - ✓ Eagle can move 48x more data in its main bus, plus additional parallelism
- **MFLOPS: EAGLE vs. ARM - the bottom line**
  - Eagle - 1,253 MFLOPS/MHz
  - ARM 10 - 2 MFLOPS/MHz
    - ✓ Eagle more than 600 times ARM performance per MHz

## MFLOPS: EAGLE vs. ARM

### EAGLE<sup>1</sup>

- 638,000 variable-length integer computations<sup>2</sup> per macroblock
- $2.29 \times 10^9$  operations<sup>2</sup> per 1280x720 pixel frame (3,600 macroblocks)
- $68.9 \times 10^9$  variable-length integer operations for 720p at 30 FPS - 68,900 MFLOPS with 55MHz clock

### ARM 10

- 2 MFLOPS/MHz
- 110 MFLOPS - running at 55MHz (Eagle's clock) - insufficient computation.
- Must run at 34 GHz to perform 68,900 MFLOPS to match Eagle. Enormous challenge.

<sup>1</sup>H.264 video compression requires only integer and no floating point calculations.

<sup>2</sup>An Eagle operation is either add/subtract/multiply/compare/select

# NOT ALL VIDEO ENCODERS ARE ALIKE

- Eagle's architecture yields the lowest possible Power Dissipation
  - Measured power in Rev. A silicon < 25 mW<sup>§</sup>
  - Measured power in Rev. B silicon < 70 mW<sup>¶</sup>
- Eagle has the shortest possible Latency
  - 698  $\mu$ s for 720p at 30fps
- **Architectural pillars behind Eagle's low power**
  - Massively parallel processing
  - Distributed memory
- An effective embodiment of true VLSI
- Eagle is truly a video encoder/compression supercomputer on a chip

§At 15 FPS – no slave mode output FIFO DRAM

¶At 30 FPS – slave mode output FIFO DRAM turned on

# APPLICATIONS TO BE ENHANCED OR ENABLED BY EAGLE'S LOW POWER AND LOW LATENCY

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- Video Camera (miniature)
- Autonomous Vehicles
- Unmanned Aerial Vehicles
- Robotics
- Wearable Electronics
- In Body Imaging
- Remote Security

- Silicon implementation without software or stored program microprocessor
- Algorithm mapped to silicon for massively parallel computation
- Distributed hierarchical memory avoids performance bottlenecks
- Encoding flexibility provided by internal registers programmable via SPI

## Granted / Issued

- US – Patent - 8,503,534 - Multi-bus architecture for a video codec; August 6, 2013
- US – Patent - 8,566,515 - Memory Subsystem; October 22, 2013
- US – Patent - 8,660,193 - Parallel, Pipelined, Integrated-Circuit Implementation of a Computational Engine; February 25, 2014
- China – Patent - ZL 2009 8 0158006.9 - Memory Subsystem; November 5, 2014
- China – Patent - ZL 2011 1 0100518.9 - Multi-bus architecture for a video codec; January 6, 2016
- China – Patent - ZL 2009 8 0158022.8 - Parallel, Pipelined, Integrated-Circuit Implementation of a Computational Engine; April 20, 2016

## Pending Applications

- Germany – Application - 11 2009 004 320.8 - Memory Subsystem; December 21, 2009
- Germany – Application - 102011002098.5 - Multi-Bus Architecture for a Video Codec; April 15, 2011
- Germany – Application - 11 2009 004 344.5 - Parallel, Pipelined, Integrated-Circuit Implementation of a Computational Engine; December 21, 2009

## ACHIEVEMENTS

- Maps the video compression algorithm directly onto the silicon
- Uses custom processors for each computational module
- Computations are tailored with the highest logic/transistor circuit efficiency
- Computation latency reduced by more than 90% over traditional computing architectures
- Silicon area is minimized
- Computations are performed with minimum power
- Allows lower internal clock frequencies making it easier to meet timing requirements

# OPTIMUM SILICON UTILIZATION

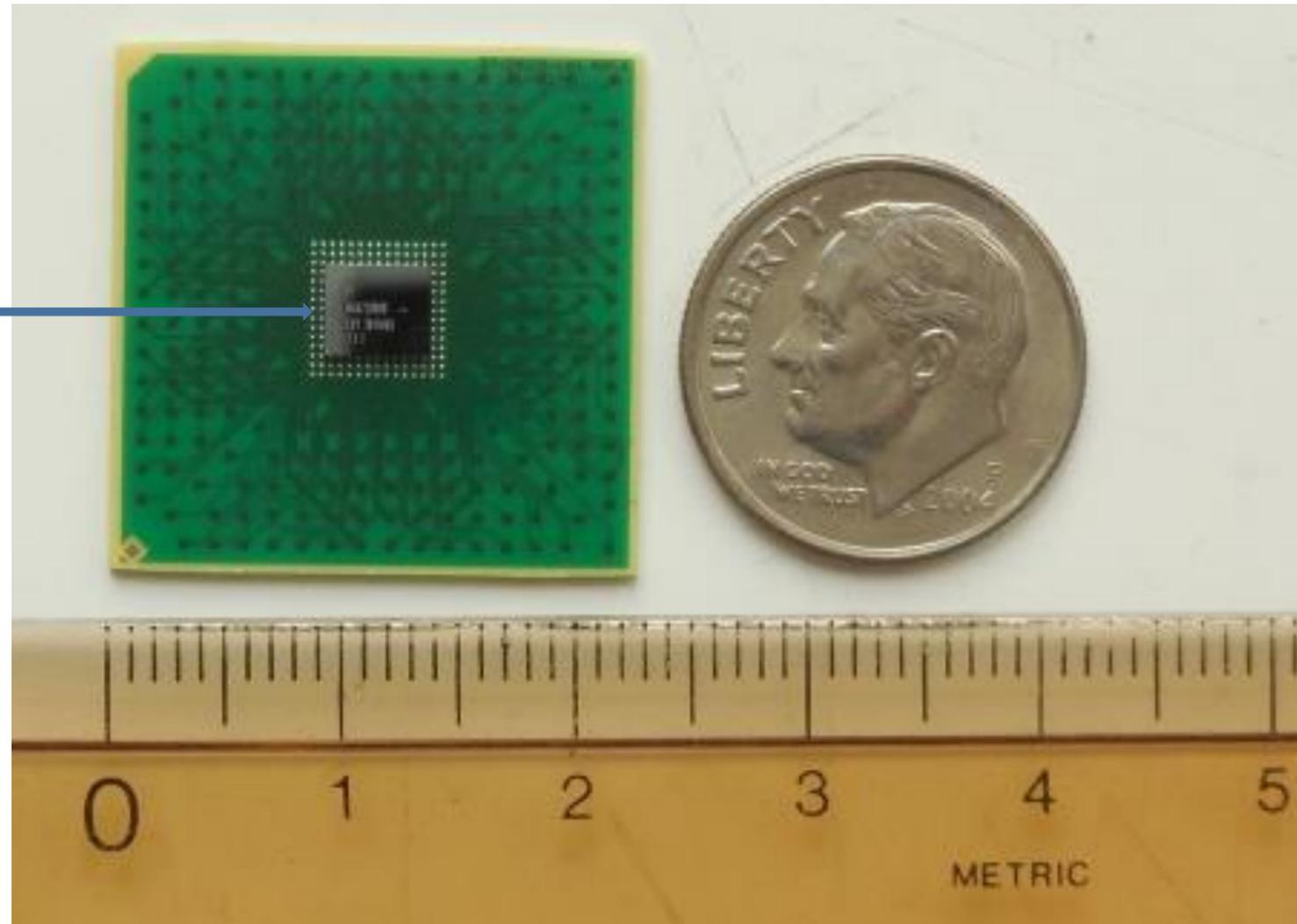
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## DEVIATIONS FROM TRADITIONAL PRACTICES

- No general purpose processors (multicore) on chip
- No silicon or power wasted in computational overhead such as instruction pre-fetch, instruction decoding, execution control in a general purpose data path
- Eliminates need to store software instructions
- Avoids the problems of performing arithmetic with circuitry designed for different word length

## EAGLE IS A TINY CHIP

Rev. B



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